REMARKS

Claims 25-41 are pending in the present application. In the office action mailed September 23, 2004 (the "Office Action"), claims 25-32, 37, and 39-41 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,027,982 to Peidous *et al.* (the "Peidous patent"). Claims 33-36 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,232,203 to Huang (the "Huang patent"). Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Peidous patent in view of U.S. Patent No. 6,265,317 to Chiu *et al.* (the "Chiu patent").

An information disclosure statement was submitted on July 15, 2003 (the "IDS"). Applicants request the Examiner consider the references cited in the Form PTO-1449 of the IDS and provide the attorney of record with a signed and initialed copy of the Form PTO-1449.

The disclosed embodiments of the invention will now be discussed in comparison to the prior art. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the prior art subject matter, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

Embodiments of the present invention are directed to a semiconductor structure, having a mask layer formed on a first layer in which a faceted or tapered opening is formed. The mask layer is typically formed from a silicon oxide material and the first layer is typically formed from a silicon nitride material. The opening in the first layer is formed over a substrate, which allows a trench to be etched into the substrate through the mask layer and the opening in the first layer. As a result, the opening in the first layer has a dimension adjacent the substrate that is approximately equal to the opening of the trench. In other embodiments of the invention, the mask layer is removed, leaving the first layer to provide a tapered opening for the trench formed in the substrate. The tapered opening through the first layer reduces the likelihood that during the deposition of an insulating material, such as a silicon oxide material, into the trench, a void will be formed. Similarly, the tapered opening through the first layer can be used for the same purpose when forming a conductive layer filling the trench.

The Peidous patent describes a method for forming a shallow trench isolation ("STI") structure. As shown in Figures 3-5 of the Peidous patent, a single etch is used to create

an opening in the thin oxide layer 34, the silicon nitride layer 33, the pad oxide layer 32. The same etch is used to form a trench 35 in the substrate 31. *See* Figures 3 and 4, and col. 3, lines 25-42. The resulting structure is then subjected to an isotropic etch that laterally removes a portion of the silicon nitride 33 sufficient to undercut the opening in the thin oxide layer 33 to create an area 36. The resulting area 36 is etched back from the opening of the trench 35 by a dimension L3. As shown in Figure 5, and described at col. 3, lines 50-53, "[a] key parameter in this process step is to time the etch such that the undercut dimension L3 is greater than or equal to the thickness dimension L4 of the silicon nitride 33." The thin oxide layer 34 is eventually etched back to provide a semiconductor structure as shown in Figure 6. In completing the STI structure, a liner oxide is formed on the exposed substrate region and in the trench to round the top corners of the trench 35, and an isolation dielectric 40 is formed over the structure to fill the remaining area in the trench and then etched back to provide the STI structure shown in Figure 11.

As previously mentioned, claims 25-32, 37, and 39-41 were rejected under 35 U.S.C. 102(b) as being anticipated by the Peidous patent.

Claims 25, 30, and 37 are patentably distinct from the Peidous patent. Claim 25 recites a semiconductor structure, comprising a trench formed in a substrate, a first layer of a first material formed over the substrate and having a faceted opening therethrough over the trench, the faceted opening having an opening over the trench approximately equal in dimensions to an opening of the trench, and a mask layer formed over the first layer and having an opening therethrough over the opening of the first layer.

Claim 30 recites a semiconductor structure, comprising a trench formed in a substrate, the trench having a trench opening dimension, and a first layer of a silicon nitride material formed over the substrate and having an faceted opening therethrough over the trench, the faceted opening having a first opening adjacent the trench having a first opening dimension and further having a second opening having a second opening dimension greater than the first opening dimension, the first opening dimension of the faceted opening approximately equal to the trench opening dimension.

Claim 37 recites a semiconductor structure, comprising a trench formed in a substrate, the trench having an opening with a trench opening dimension, a mask layer having an

opening therethrough and located over the trench, the opening in the mask layer having a mask layer opening dimension, and a first layer interposed between the substrate and the mask layer, the first layer having an opening undercutting the opening of the mask layer, the opening in the first layer having a dimension adjacent the substrate approximately equal to the trench opening dimension.

Claims 25, 30, and 37 are patentably distinct from the Peidous patent because the Peidous patent fails to disclose the combination of limitations recited by the respective claims. For example, the Peidous patent fails to at least disclose a faceted opening in the first layer and over the trench that has a dimension adjacent the trench approximately equal in dimension to an opening of the trench. The Peidous patent further fails to disclose an opening in the first layer having a first opening adjacent the trench with a first opening dimension approximately equal to the dimension of the trench opening and further having a second opening with a second opening dimension greater than the first opening dimension. The Peidous patent does not disclose the combination of limitations recited by claims 25, 30, and 37 because a single etch step is used to form an opening through the thin oxide layer 34, the silicon nitride layer 33, the pad oxide layer 32, and to form the trench 35 in the substrate, as previously discussed. The opening in the silicon nitride layer 33 is not used with the opening in a mask layer to define the opening of trench formed during a subsequent etch process. Consequently, the opening in the silicon nitride layer 33 does not have a dimension adjacent the substrate that is approximately equal to the opening of the trench. In fact, as described in the Peidous patent, it is "key" that the area 36 created by the isotropic etch has an etch back dimension L3 that exceeds the thickness of the silicon nitride layer L4. As shown in Figure 5 of the Peidous patent, this key aspect of the formation of the STI structure is ensured by etching the opening in the silicon nitride layer 33 to have a dimension adjacent the substrate 31 that is much greater than the dimension of the opening of the trench 35.

For the foregoing reasons, claims 25, 30, and 37 are patentably distinct from the Peidous patent. Claims 26-29, which depend from claim 25, claims 31 and 32, which depend from claim 30, and claims 39-41, which depend from claim 37, are similarly patentably distinct based on their dependency from a respective allowable base claim. That is, each of the dependent claims further narrows the scope of the claim from which it depends, and

consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable. Therefore, the rejection of claims 25-32, 37, and 39-41 under 35 U.S.C. 102(b) should be withdrawn.

As previously mentioned, claims 33-36 are rejected under 35 U.S.C. 102(b) as being anticipated by the Huang patent. Claim 33 recites a semiconductor structure, comprising a trench formed in a substrate, the trench having an opening with a trench opening dimension, and a first layer of a silicon nitride material formed over the substrate and having a first side proximate to the substrate and a second side opposite of the first side, and further having an opening therethrough over the trench, the opening undercuts an opening in a mask layer and has a first dimension along the first side approximately equal to the trench opening dimension and a second dimension along the second side greater than the first dimension.

Claim 33 is patentably distinct from the Huang patent because the Huang patent fails to disclose the combination of limitations recited by claim 33. For example, the Huang patent fails to at least disclose an opening through a first layer of silicon nitride material that undercuts a mask layer and has a first dimension along a first side approximately equal to the trench opening dimension and further having a second dimension along a second side greater than the first dimension. The Huang patent is directed to forming a STI structure employing nitride spacers 18a/18b along the upper edges of a trench 8 in order to reduce oxide loss at these edges. According to the Huang patent, the loss of oxide at the top corners of the trench results in greater parasitic current. The nitride spacers formed over these corners prevent oxide loss during subsequent etching steps in the formation of the STI structure. The formation of the trench in the Huang patent is, as with the Peidous patent, formed during the same etch process that is used to form openings through a silicon nitride layer 14 and a pad oxide layer 12. The opening through the silicon nitride layer does not undercut a mask layer and does not have a first dimension along a first side that is greater than a second dimension along a second side.

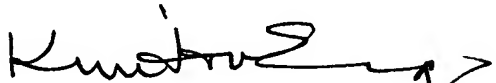
For the foregoing reasons, claim 33 is patentably distinct from the Peidous patent. Claims 34-36, which depend from claim 33, are similarly patentably distinct based on their dependency from a respective allowable base claim. Therefore, the rejection of claims 33-36 under 35 U.S.C. 102(b) should be withdrawn.

Claim 38 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Peidous patent in view of the Chiu patent. Claim 38 is allowable because of its dependency from allowable claim 37, as well as the fact that the combined teachings of the Peidous and Chiu patents fail to teach or suggest the combination of limitations recited by claim 38. That is, even if it is assumed that the Chiu patent teaches the subject matter as characterized by the Examiner, it fails to make up for the deficiencies in the Peidous patent as previously discussed with respect to claims 25, 30, and 37. Therefore, the rejection of claim 38 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



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